

INTRODUCTION

The CCD65 is part of the new L3Vision[®] range of products from e2v technologies. This device uses a novel output amplifier circuit that is capable of operating at an equivalent output noise of less than one electron at pixel rates of over 11 MHz (corresponding to a field rate of 50 Hz). This makes the sensor well suited for scientific imaging where the illumination is limited or for video applications at very low light levels.

The sensor is a frame transfer device and operates in inverted mode to suppress dark current as this is now the dominant noise source (even at 50 Hz field rate).

The multiplication gain may be varied by adjustment of the multiplication phase amplitude $R\phi/2HV$.

The device functions by converting photons to charge in the image area during the integration time period, then transferring this charge through the image and store sections into the readout register. Following transfer through the readout register, the charge is multiplied in the gain register prior to conversion to a voltage by a low noise output amplifier.

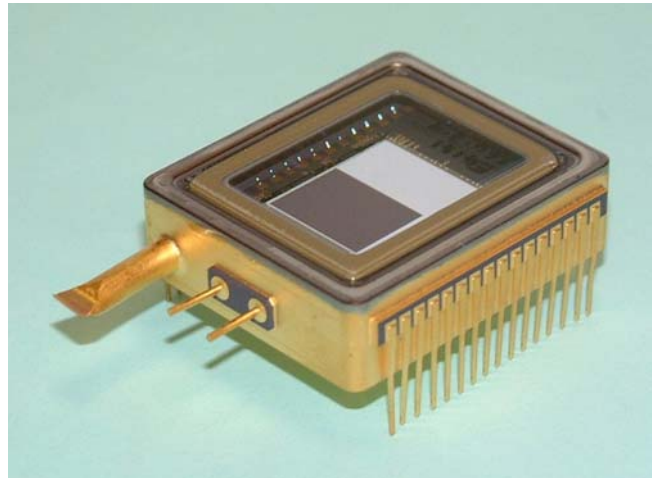
Variants exist to provide the following options:

- Optional anti-blooming
- 525- or 625-line format

Note that e2v technologies also supply modules for operating devices at TV rates.

GENERAL DATA

Active image area	11.52 x 8.64 mm
Image section active pixels:	
625-line	576 (H) x 288 (V)
525-line	576 (H) x 244 (V)
Image pixel size:	
625-line	20 x 30 μ m
525-line	20 x 35.5 μ m
Number of output amplifiers	1
Fill factor (for non-antibloomed devices)	100%
Additional dark reference columns	15
Additional overscan rows:	
625-line	8
525-line	6
Spectral range	400 - 1060 nm



PACKAGE DETAILS (Nominal, see Fig. 19)

Peltier Cooled Package

Overall dimensions	34.2 x 30.48 mm
Number of pins	32
Inter-pin spacing	1.778 \pm 0.130 mm
Opposite row spacing	30.48 mm
Window material	sapphire
Mounting position	any
Height of active surface above base	6.5 \pm 0.4 mm

STORAGE AND OPERATION TEMPERATURE EXTREMES

	MIN	MAX
Storage temperature ($^{\circ}$ C)	-55	+125
Operating temperature ($^{\circ}$ C)	-55	+60
Temperature ramping ($^{\circ}$ C/min)	-	5

Users wishing to operate the device outside this range are advised to consult e2v technologies.

TYPICAL PERFORMANCE SPECIFICATIONS

The following are specified for standard 625-line, 50 Hz operating mode at typical operating voltages. Parameters are given at 293 K unless specified otherwise. Where parameters differ in normal and high gain modes, both are given. Where parameters differ for 525-line, 60 Hz operation, this figure is stated in brackets.

PARAMETER	UNIT	MIN	TYPICAL	MAX
Output amplifier responsivity (normal mode)	$\mu\text{V}/e^-$	-	1.0	-
Multiplication register gain (see notes 1, 2 and 3)		1	-	1000
Peak signal - non-antiblooming (normal mode)	e^-/pixel	100k	250k (290k)	-
Peak signal - antiblooming (normal mode)	e^-/pixel	60k	150k (170k)	-
Charge handling capacity of gain register	e^-/pixel	-	600k	-
Peak output voltage (normal mode)	V	-	0.25 (0.29)	-
Peak output voltage (high gain mode)	V	-	0.6	-
Readout noise at 50 Hz (normal mode) (see notes 4 and 5)	$e^- \text{ rms}$	-	100	-
Readout noise at 50 Hz (high gain mode) (see note 4)	$e^- \text{ rms}$	-	< 1	-
Dark signal at 293 K (see note 6)	$e^-/\text{pixel/s}$	-	290 (340)	500
Dark signal non-uniformity (DSNU) at 293 K (see notes 5 and 7)	$e^-/\text{pixel/s}$	-	120 (140)	-
Dark signal at 273 K (see note 6)	$e^-/\text{pixel/s}$	-	40 (50)	80
Dark signal non-uniformity (DSNU) at 273 K (see notes 5 and 7)	$e^-/\text{pixel/s}$	-	16 (20)	-
Dynamic range (see note 8)		-	see note 8	-
Excess noise factor (see note 9)		-	$\sqrt{2}$	-
Maximum parallel transfer frequency	MHz	-	-	1

NOTES

1. The typical dependence of gain on $R\text{Ø}2\text{HV}$ is shown in Fig. 1.
2. The variation of gain with $R\text{Ø}2\text{HV}$ at different temperatures is shown in Fig. 1.
3. Some increase of $R\text{Ø}2\text{HV}$ may be required throughout life to maintain gain performance. Adjustment of $R\text{Ø}2\text{HV}$ should be limited to the maximum specified under Operating Conditions.
4. A frame rate of 50 Hz corresponds to 625-line TV operation (a pixel rate of 11 MHz).
5. These noise values are dominated by reset noise in the output amplifier and it is assumed that correlated double sampling (CDS) is not being employed. If CDS is used to suppress the reset component, a noise of $10 e^-$ can typically be achieved at a pixel rate of 1 MHz with a noise floor of $4 e^- \text{ rms}$. At 11 MHz TV rate the noise with CDS is about $35 e^-$ and, assuming a 20 pF load, the output will be settled to 1%. These values are inferred by design and not measured.
6. For the variation of dark signal with temperature, refer to Fig. 2. The dark signal has the usual temperature dependent component and an additional weakly temperature dependent component, which is independent of the integration time.
7. DSNU is defined as the 1σ variation of the dark signal.
8. Dynamic range is defined as the maximum output signal divided by the total noise referenced to the input of the readout register. As gain is increased, the effective readout noise decreases with a consequential increase in dynamic range. This improvement continues until the pixel full well with applied gain exceeds the charge handling capacity of the gain register. This is illustrated in Fig. 3 for an output amplifier noise of $100 e^-$.
9. The excess noise factor is defined as the factor by which the multiplication process increases the shot noise on the image when multiplication gain is used.

DEVICE COSMETIC PERFORMANCE

Grade 1 devices are supplied to the blemish specification shown below.

Note that incorrect biasing of the device may result in spurious dark or white blemishes appearing. These will be eliminated if the biases are adjusted.

Test Conditions

Operating mode	Device run in standard 2-phase interlace TV mode (50 Hz field rate for 625-line devices, 60 Hz field rate for 525-line devices).
Sensor temperature	-5 ± 3 °C.
Multiplication gain	Set to approximately 1000.
Illumination	Set to give a signal level of approximately $50 e^-$ /pixel/field (roughly corresponding to quarter moonlight scene illumination through an f/1.4 lens).

BLEMISH SPECIFICATION

Black Columns Black defects are counted when they have a responsivity of less than 80% of the local mean signal at approximately the specified multiplication gain and level of illumination. A black column contains at least 9 contiguous black defects.

White Columns White defects are pixels having a dark signal generation rate corresponding to an output signal of greater than 5% of multiplication register capacity at a gain of 1000. A white column contains at least 9 contiguous white defects.

Pin-Head Columns Pin-head columns are manifest as a partial dark column with a bright pixel showing photoresponse at the end of the column nearest to the readout register. Pin-head columns are counted when the black column has a responsivity of less than 80% of the local mean signal at approximately the specified multiplication gain and level of illumination. A pin-head column contains at least 9 black defects.

SPECIFICATION FOR GRADE 1 DEVICES

PARAMETER	SPECIFICATION
White Columns	0
Black Columns	0
Pin-head Columns	0

ORDERING INFORMATION

PART NUMBER	FORMAT	OPERATING MODE	ANTIBLOOMING	WINDOW
CCD65-06-* -428	625-line	IMO	Shielded	Permanent
CCD65-05-* -427	525-line	IMO	Shielded	Permanent
CCD65-05-* -B93	525-line	IMO	None	Permanent
CCD65-06-* -B94	625-line	IMO	None	Permanent

Figure 1: TYPICAL VARIATION OF MULTIPLICATION GAIN WITH $R\phi 2HV$ AT DIFFERENT TEMPERATURES

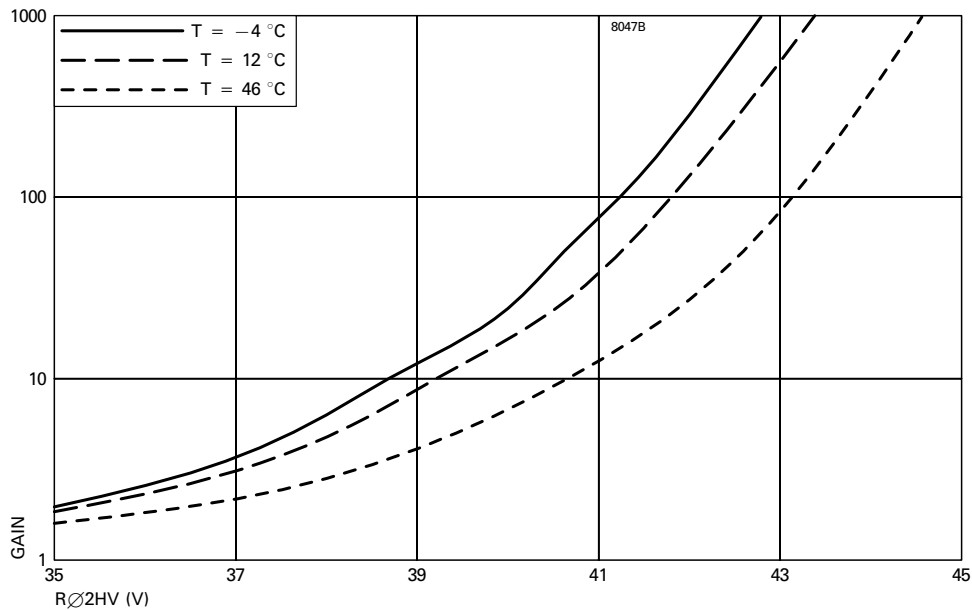


Figure 2: TYPICAL VARIATION OF DARK SIGNAL WITH TEMPERATURE

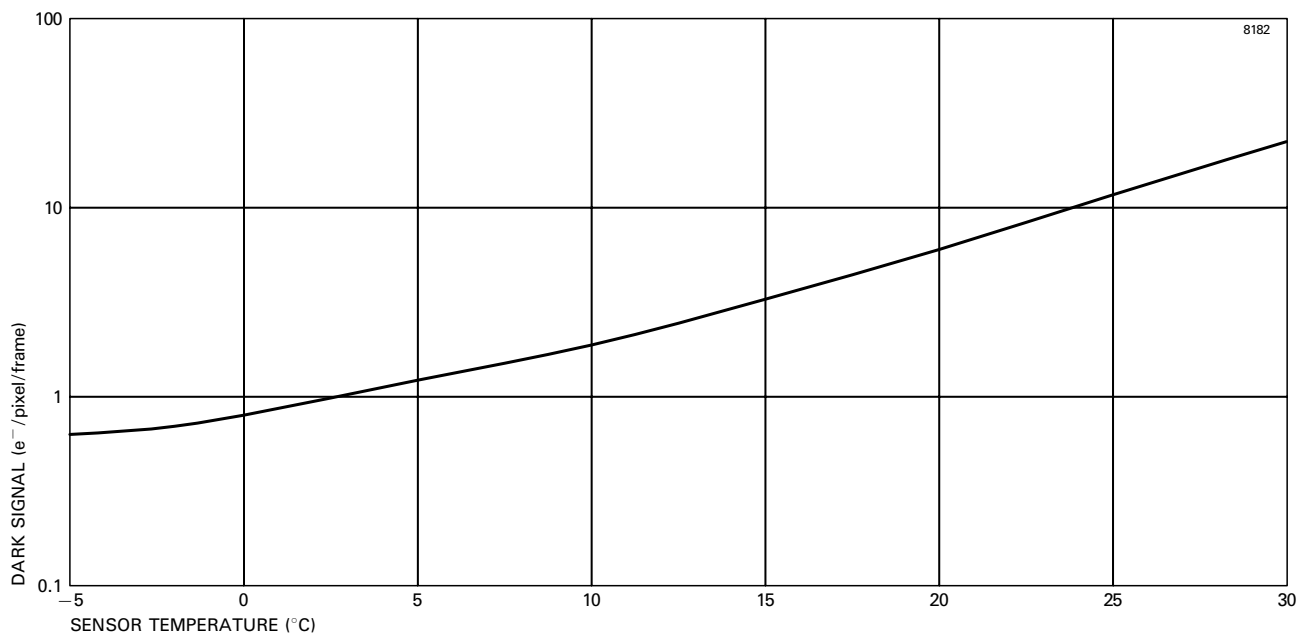


Figure 3: TYPICAL VARIATION OF INTRA-SCENE DYNAMIC RANGE WITH GAIN (Non-antibloomed)

Assumed amplifier noise = $100 e^-$ rms (no CDS). See note 8 for the definition of dynamic range.

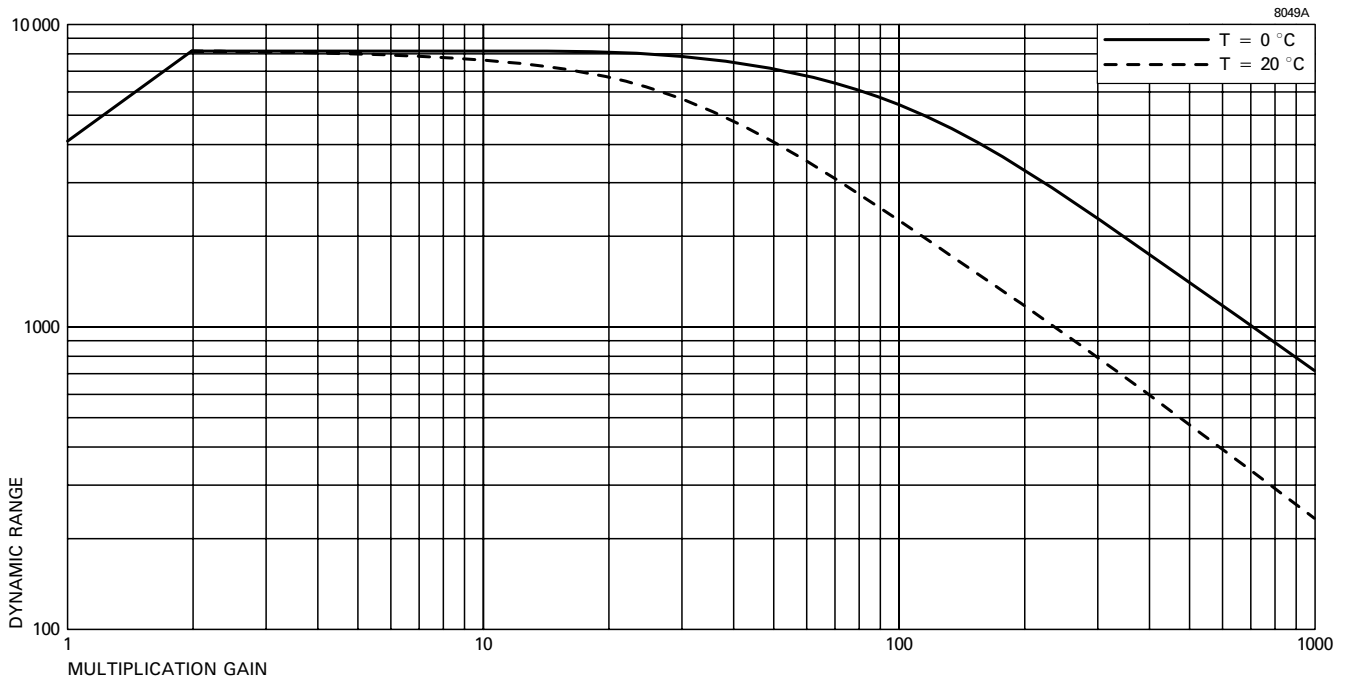


Figure 4: TYPICAL SPECTRAL RESPONSE OF ANTIBLOOMED AND NON-ANTIBLOOMED DEVICES AT $T = 20^\circ\text{C}$

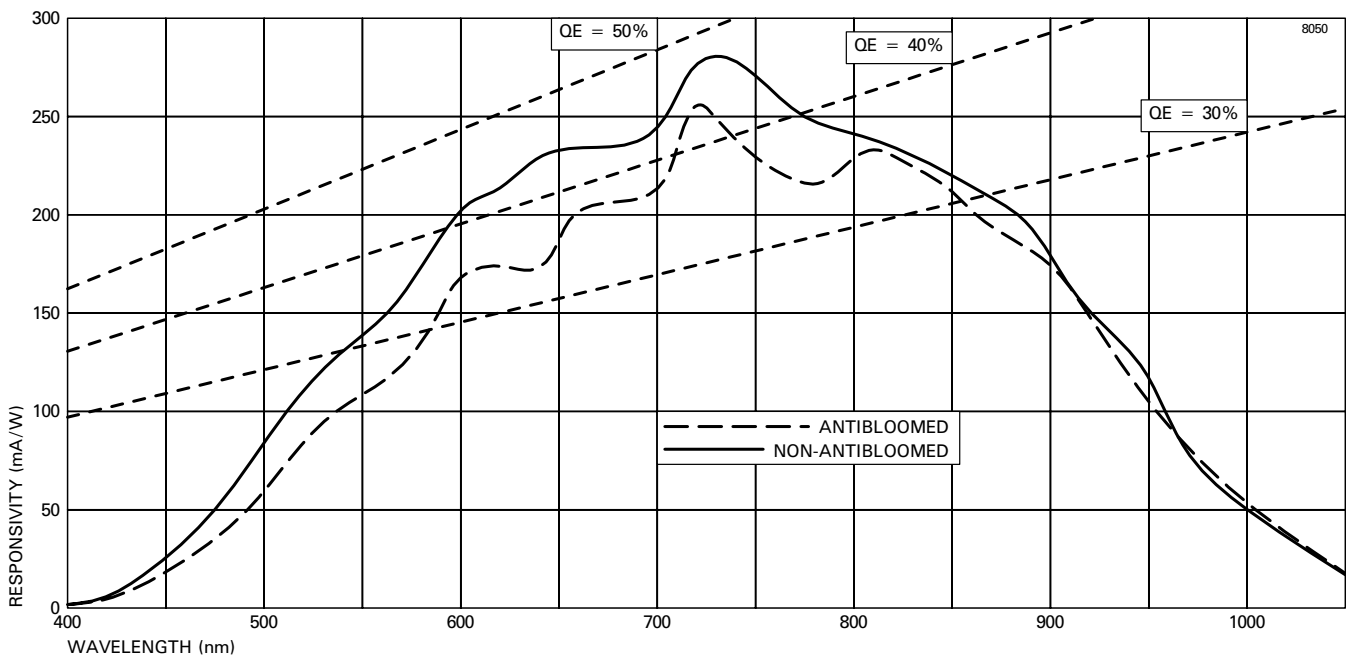


Figure 5: TYPICAL HORIZONTAL RESOLUTION

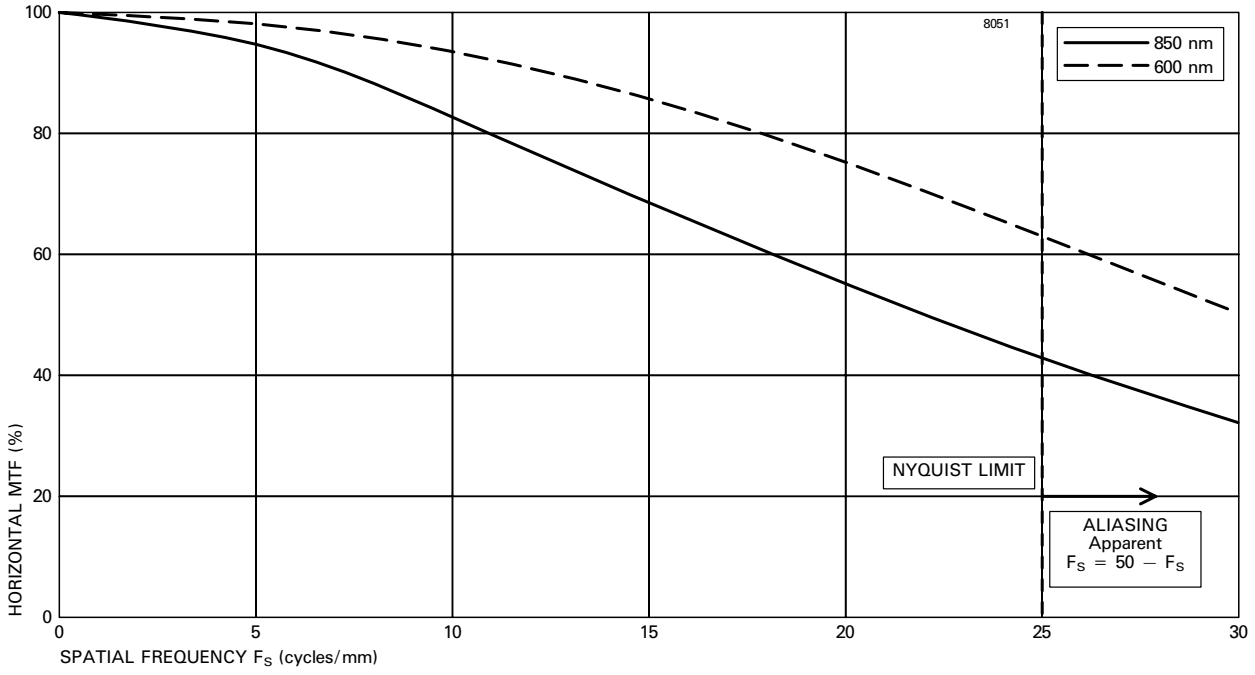
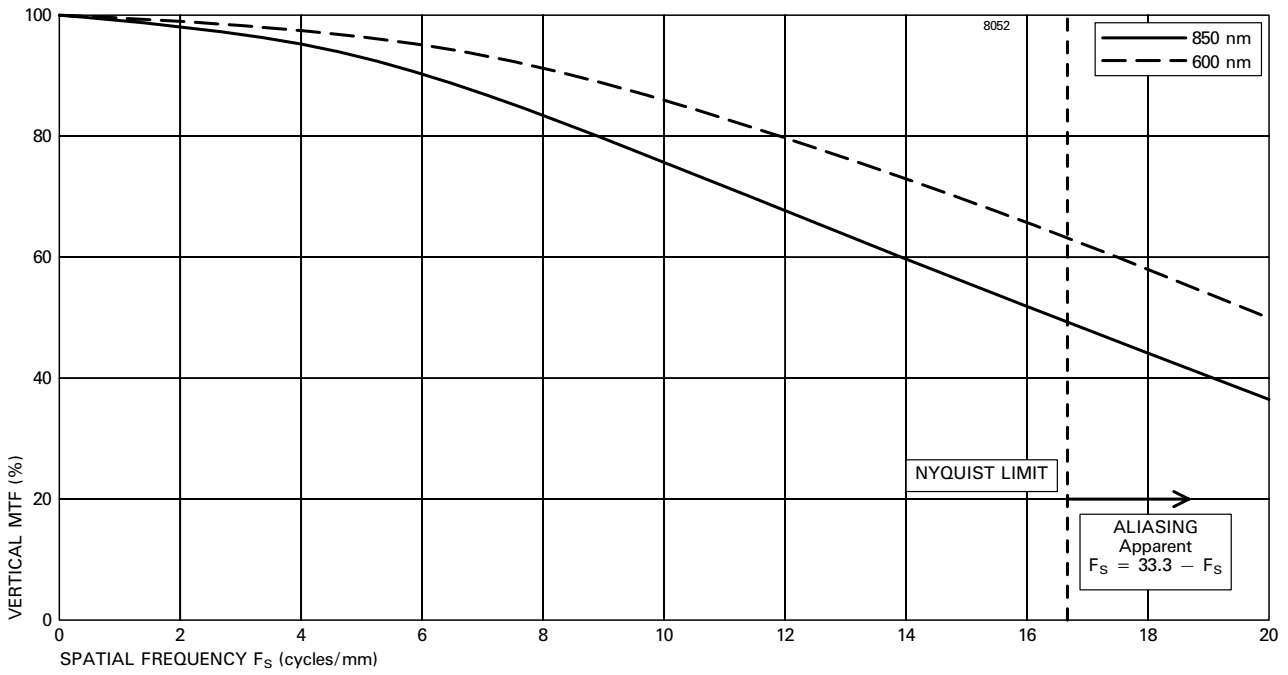


Figure 6: TYPICAL VERTICAL RESOLUTION
Vertical MTF shown for 625-line devices



ABSOLUTE MAXIMUM RATINGS

Maximum ratings are with respect to SS.

PIN	CONNECTION	MIN (V)	MAX (V)
1	n.c.		
2	n.c.		
3	n.c.		
4	n.c.		
5	Thermistor		
6	SS	0	
7	IØ1	-20	+20
8	ABD	-0.3	+25
9	SØ1	-20	+20
10	SØ2	-20	+20
11	RØ2HV	-20	+50
12	RØDC	-20	+20
13	DD	-0.3	+25
14	GD	-0.3	+25
15	OG	-20	+20
16	RD	-0.3	+25
17	ØR	-20	+20
18	DOD	-0.3	+32
19*	DOS	-0.3	+25
20*	OS	-0.3	+25
21	OD	-0.3	+32
22	RØ3	-20	+20
23	RØ1	-20	+20
24	RØ2	-20	+20
25	ABG	-20	+20
26	IØ2	-20	+20
27	SS	0	
28	Thermistor		
29	n.c.		
30	n.c.		
31	n.c.		
32	n.c.		

n.c. = not connected.

* Permanent damage may result if, in operation, OS or DOS experience short circuit conditions.

Maximum voltages between pairs of pins:

PIN	CONNECTION	PIN	CONNECTION	MIN (V)	MAX (V)
21	OD	20	OS	-15	+15
18	DOD	19	DOS	-15	+15
11	RØ2HV	12	RØDC	-20	+50
11	RØ2HV	22	RØ3	-20	+50
Maximum Peltier current (A)					6
Output transistor current (mA)					20

OPERATION OF PELTIER COOLER

Operating the device at TV rate, with the heat extracted from the base of the package using a 1 °C/W heatsink to an ambient temperature of 30 °C, cooling the sensor to -10 °C will typically require a Peltier supply current of approximately 3 A and a potential of approximately 1 V.

THERMISTOR

The package includes a Fenwal thermistor for temperature sensing, part number 196-302LAD-002.

ESD HANDLING PROCEDURES

CCD sensors, in common with most high performance IC devices, are static sensitive. In certain cases a static electricity discharge may destroy or irreversibly degrade the device. Accordingly, full anti-static handling precautions should be taken whenever using a CCD sensor or module. These include:

- Working at a fully grounded workbench.
- Operator wearing a grounded wrist strap.
- All receiving socket pins to be positively grounded.
- Unattended CCDs should not be left out of their conducting foam or socket.

All devices are provided with internal protection circuits to most gate electrodes but not to the other pins.

Evidence of incorrect handling will terminate the warranty.

EXPOSURE TO RADIATION

Exposure to radiation may irreversibly damage the device and result in degradation of performance. Users wishing to operate the device in a radiation environment are advised to consult e2v technologies.

OPERATING CONDITIONS

Typical operating voltages are as given in the table below. Some adjustment within the minimum-maximum range specified may be required to optimise performance.

CONNECTION	PULSE AMPLITUDE OR DC LEVEL (V)		
	Min	Typical	Max
IØ1,2 high	+5 (see note 10)	+7	+9 (see note 10)
IØ1,2 low	-	-5	-
SØ1,2 high	+5 (see note 10)	+7	+9 (see note 10)
SØ1,2 low	-	-5	-
RØ1,2,3 high	+10	+12	+13
RØ1,2,3 low	-	0	-
RØ2HV high	+20	+40	+50 (see note 3)
RØ2HV low	0	+4	-
ØR high	see note 11	+10	see note 11
ØR low	-	0	-
RØDC	+2	+4	+5
OG	+1	+3	+5
ABG	-	0	-
SS	0	+4.5	+7
OD, DOD	+25	+28	+32
RD	+15	+18	+20
ABD	+10	+15	+20
GD	+15	+23	+25
DD	+20	+24	+25

NOTES

10. IØ and SØ adjustment may be common.
 11. ØR high level may be adjusted in common with RØ1,2,3.

An external load is required. This can either be a resistor of about 2 kΩ (non-critical) or a constant current type of about 10 mA. The total on-chip power dissipation is in the range 300 - 400 mW, depending on the details of the voltages and clock timings used.

DRIVE PULSE WAVEFORM SPECIFICATION

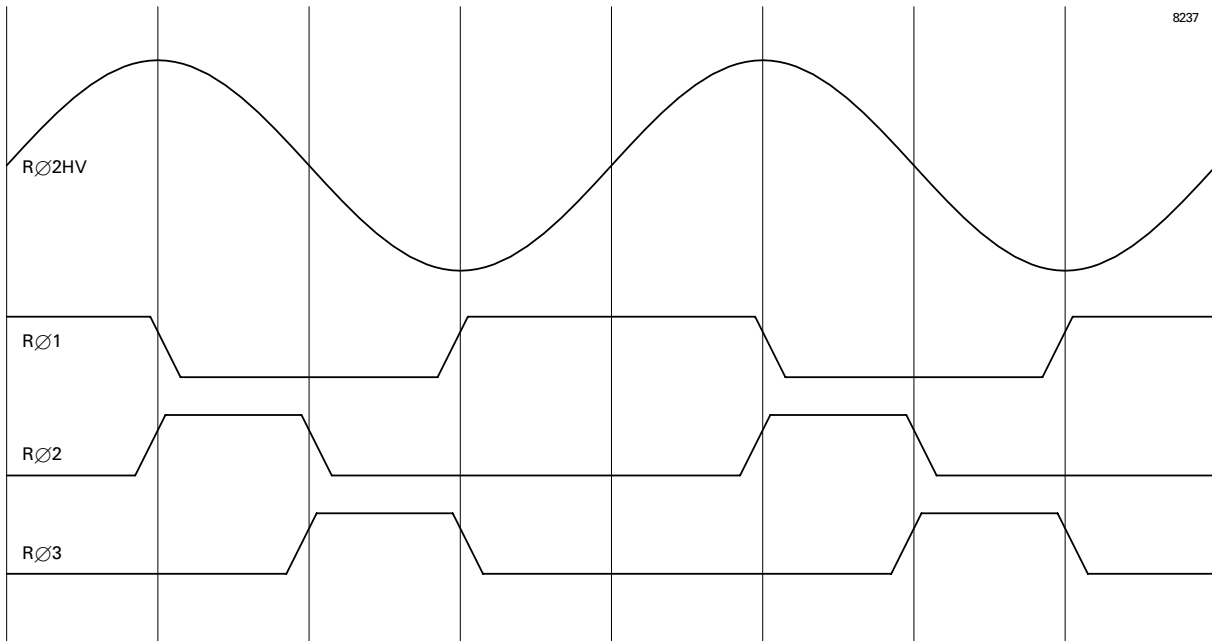
The following are suggested pulse rise and fall times.

CLOCK PULSE	TYPICAL RISE TIME (ns)	TYPICAL FALL TIME (ns)	TYPICAL PULSE OVERLAP
IØ	30	30	@90% points
SØ	30	30	@90% points
RØ1	10	10	@70% points
RØ2	10	10	@70% points
RØ3	10	10	@70% points
RØ2HV	25	25	see note 13
RØ2HV	Sine	Sine	Sinusoid- high on falling edge of RØ1

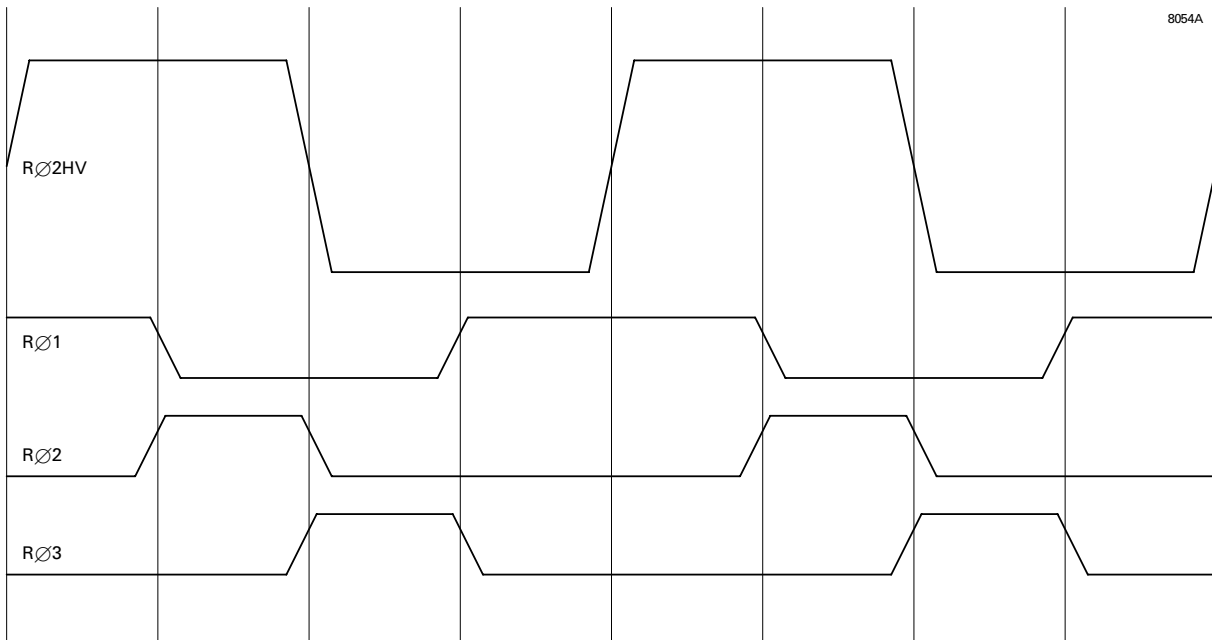
NOTES

12. Register clock pulses are as shown in the line timing diagram, Fig. 11.
 13. An example clocking scheme is shown in Fig. 7. RØ2HV can also be operated with a normal clock pulse, as shown in Fig. 8. The requirement for successful clocking is that RØ2HV reaches its maximum amplitude before RØ1 goes low.

**Figure 7: CLOCKING SCHEME FOR MULTIPLICATION GAIN
(Sine wave clocking scheme)**

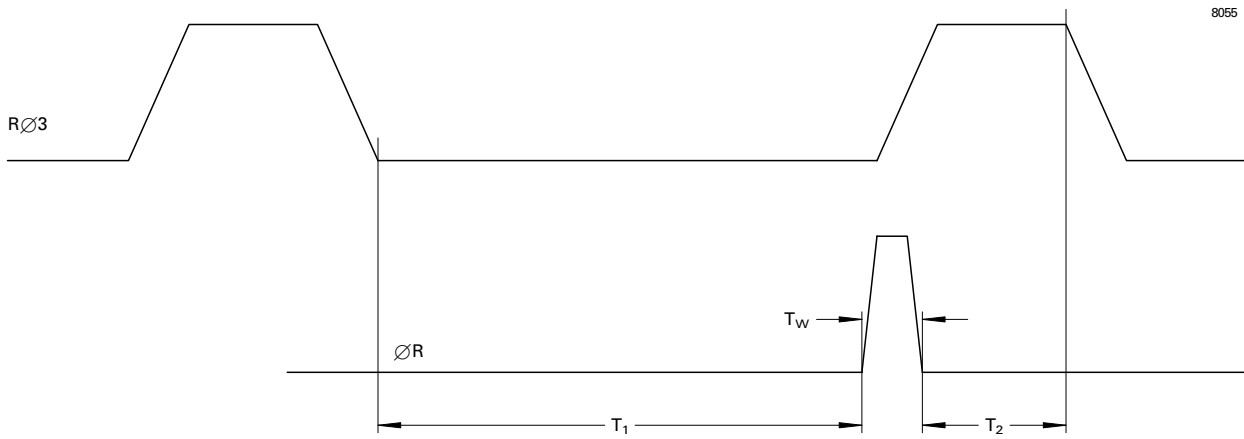


**Figure 8: CLOCKING SCHEME FOR MULTIPLICATION GAIN
(Conventional clocking scheme)**



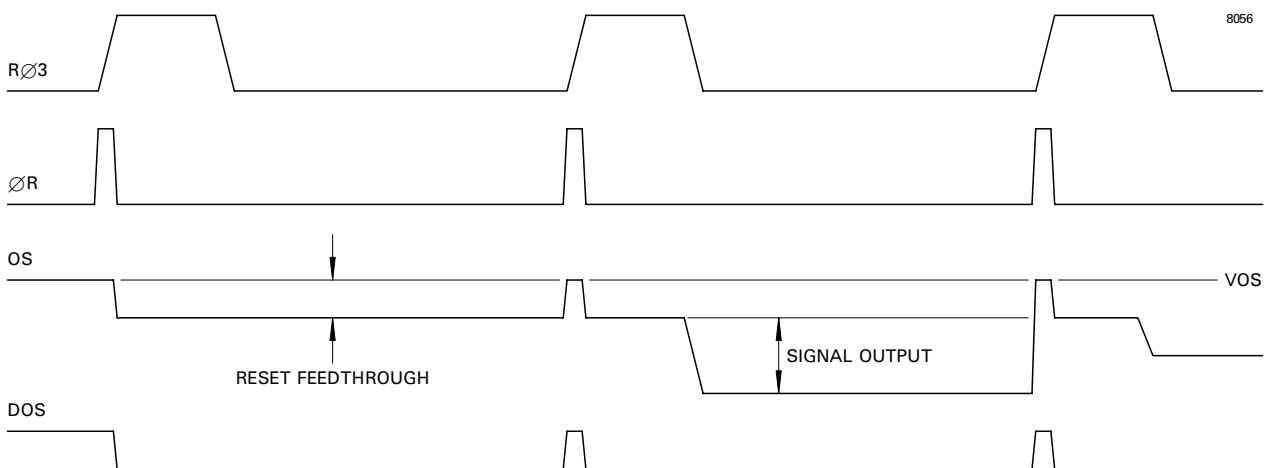
PULSE TIMINGS AND OVERLAPS

Figure 9: RESET PULSE



$T_w = 10 \text{ ns typical}$
 $T_1 = \text{output valid}$
 $T_2 > 0 \text{ ns}$

Figure 10: PULSE AND OUTPUT TIMING



ELECTRICAL INTERFACE CHARACTERISTICS

ELECTRODE CAPACITANCES AT MID CLOCK LEVELS				
Connection	Capacitance to SS	Inter-phase Capacitances	Total Capacitance	Units
IØ1	10	1	11	nF
IØ2	10	1	11	nF
SØ1	7.5	1	8.5	nF
SØ2	7.5	1	8.5	nF
RØ1	45	73	118	pF
RØ2	32	41	73	pF
RØ3	67	70	137	pF
RØ2HV	35	45	80	pF
SERIES RESISTANCES				
Connection	Approximate Total Series Resistance			
IØ1	12			Ω
IØ2	12			Ω
SØ1	14			Ω
SØ2	14			Ω
RØ1	6			Ω
RØ2	6			Ω
RØ3	6			Ω
RØ2HV	8			Ω
APPROXIMATE OUTPUT IMPEDANCE				
Large Signal Amplifier	250			Ω

Figure 11: LINE TIMING DIAGRAM (625-line TV)

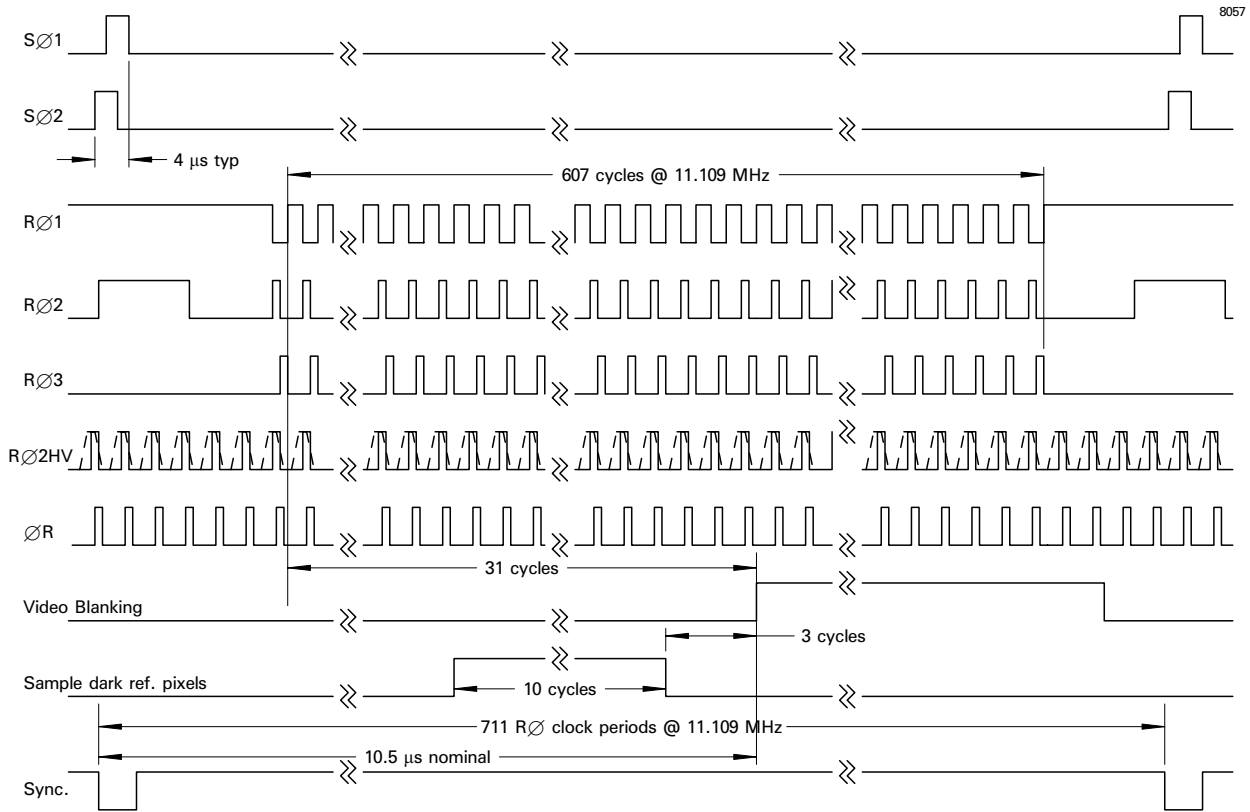


Figure 12: FRAME TIMING DIAGRAM (625-line TV)

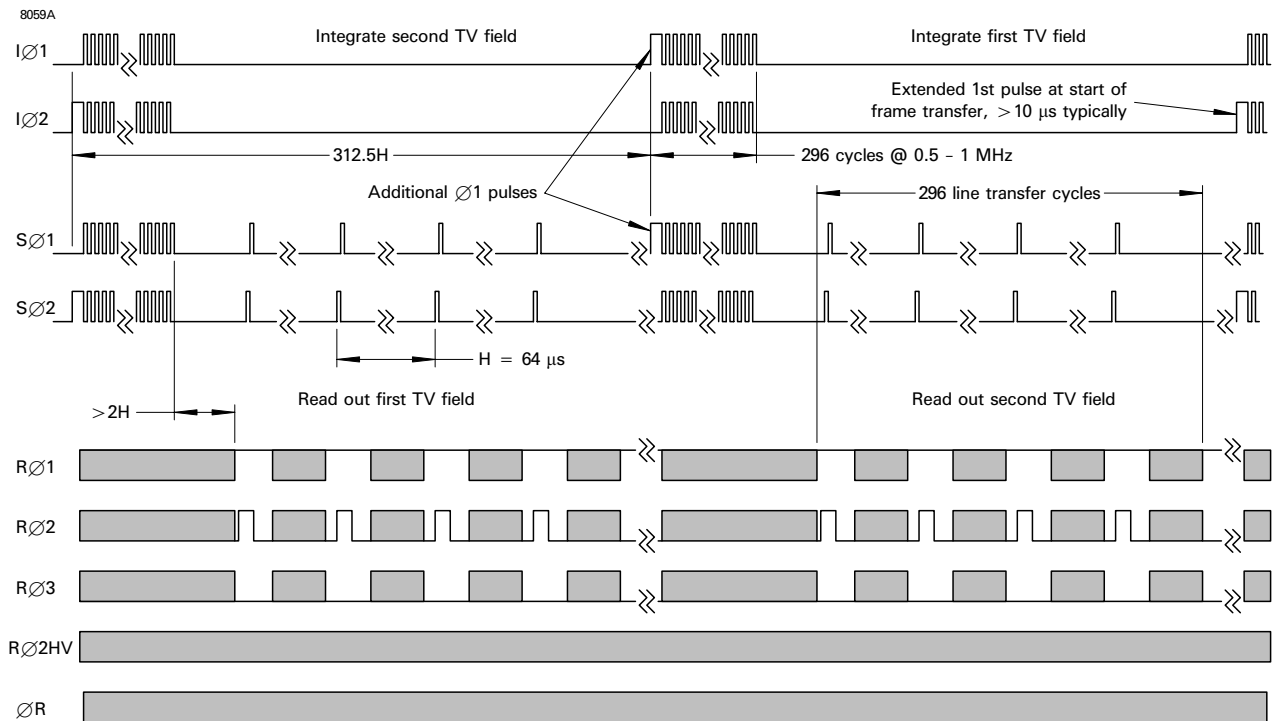


Figure 13: LINE TIMING DIAGRAM (525-line TV)

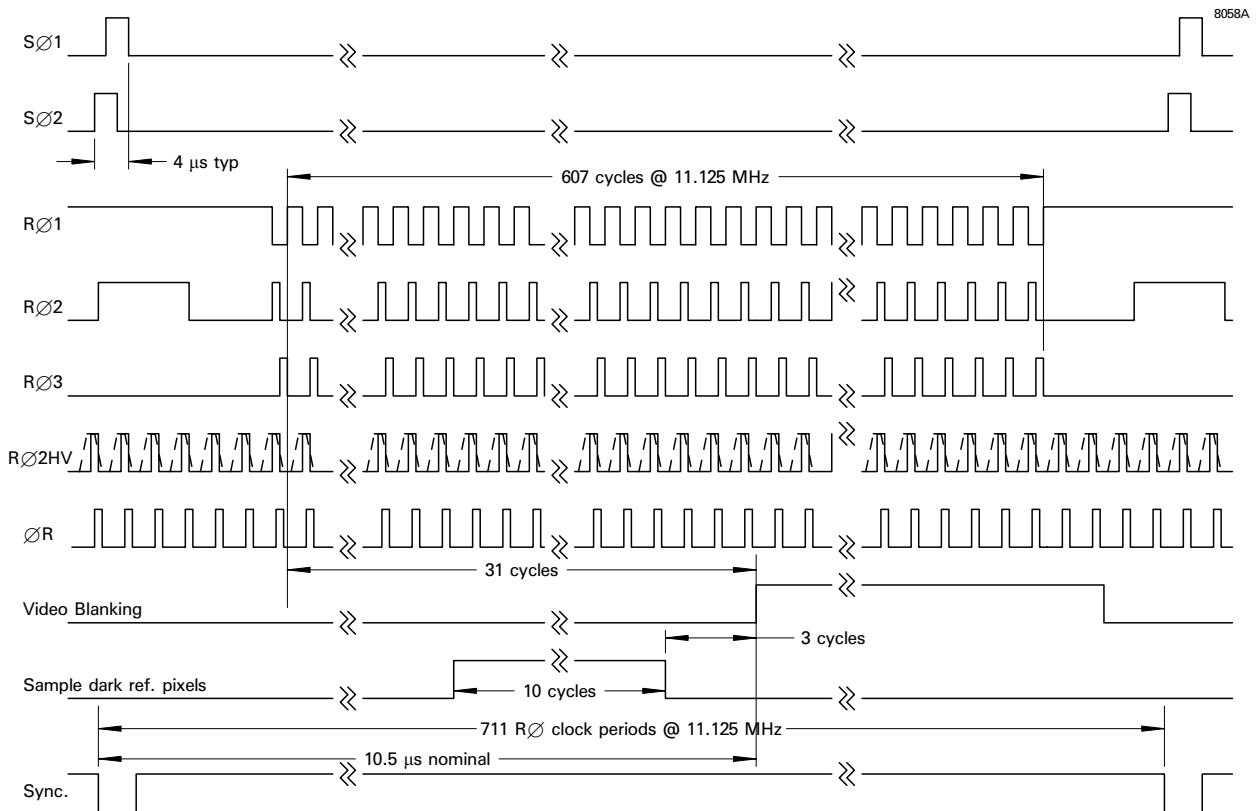


Figure 14: FRAME TIMING DIAGRAM (525-line TV)

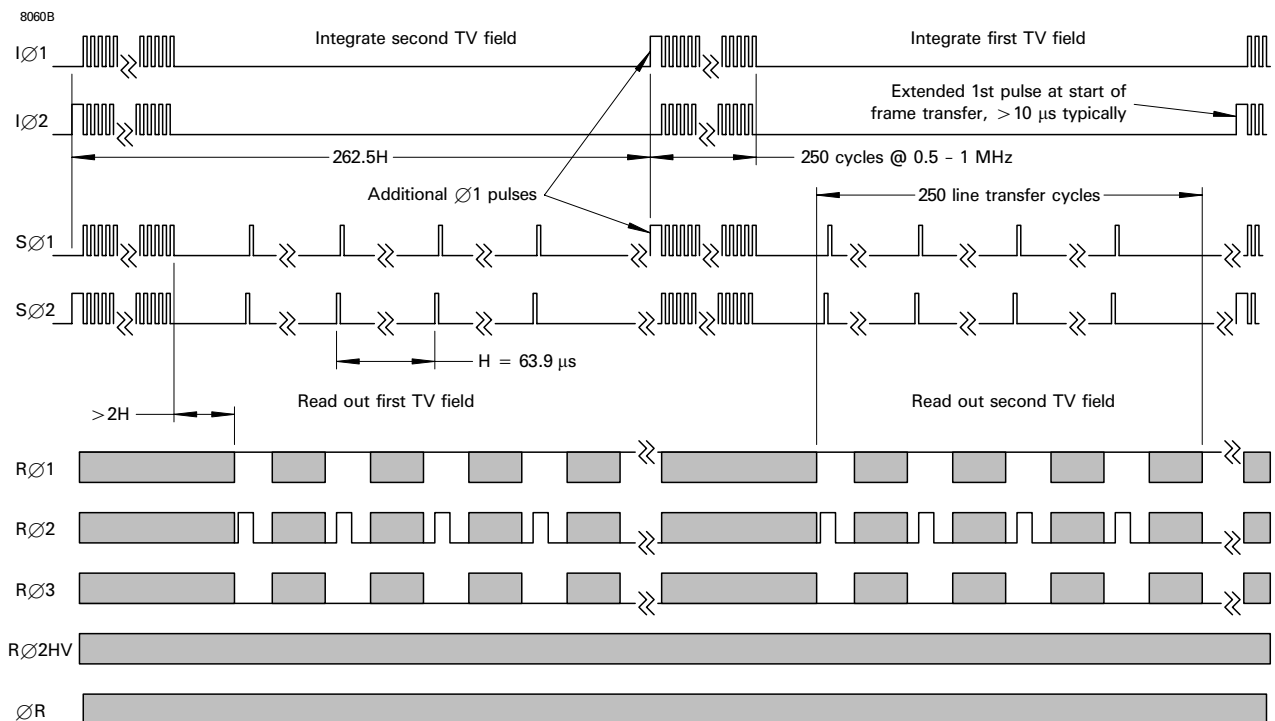
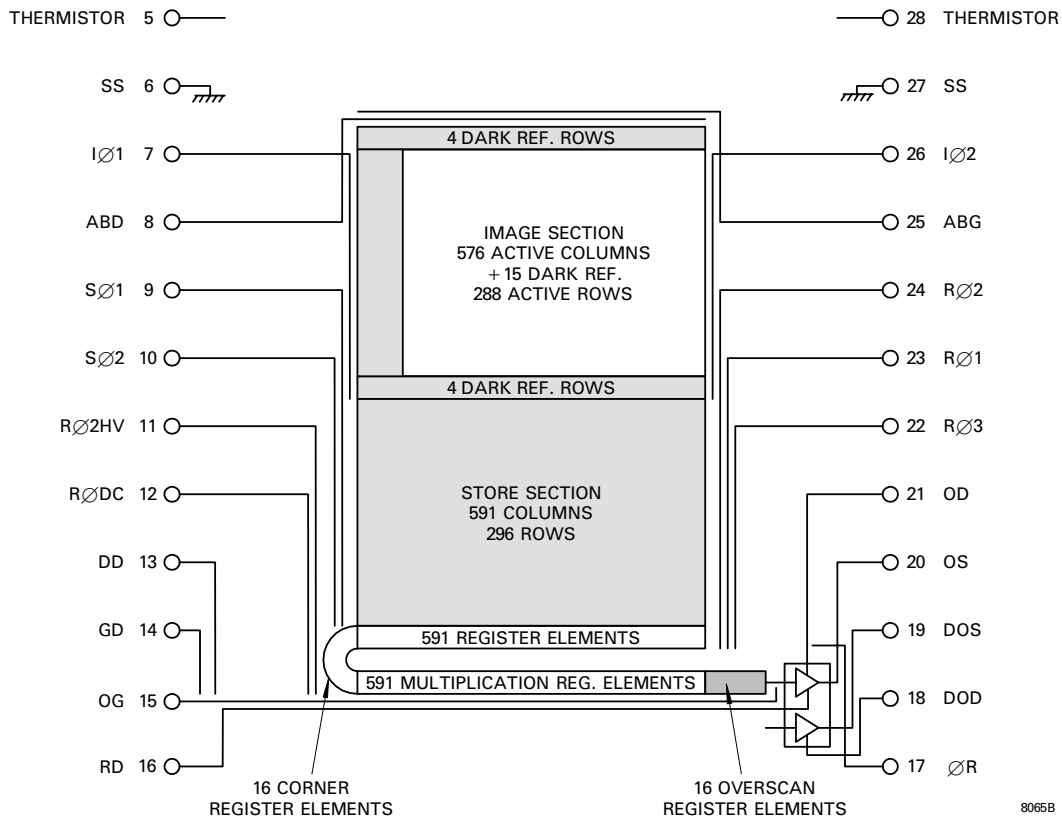
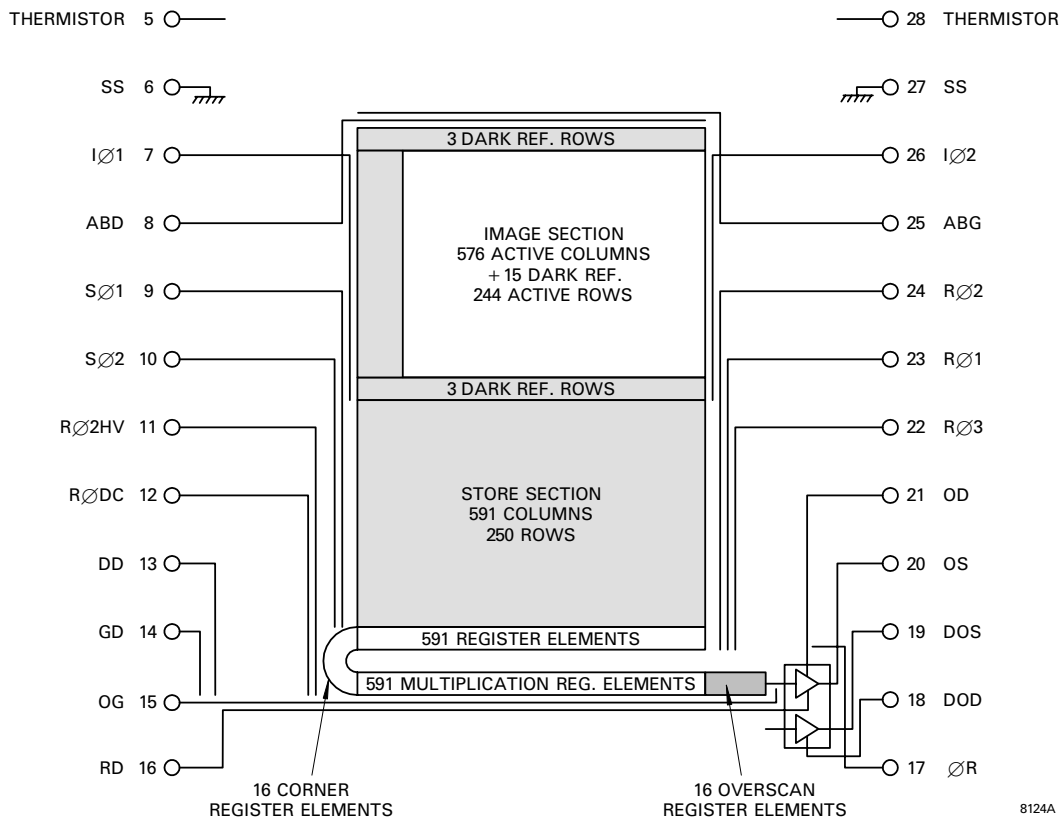


Figure 15: SCHEMATIC CHIP DIAGRAM (625-line)



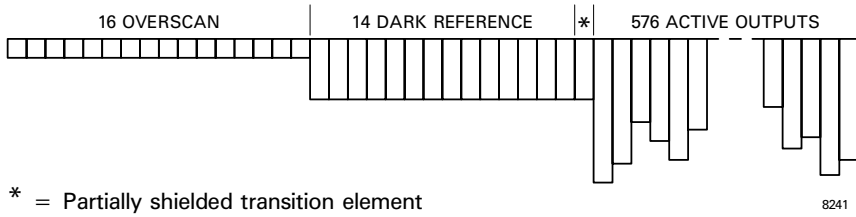
8065B

Figure 16: SCHEMATIC CHIP DIAGRAM (525-line)



8124A

Figure 17: LINE OUTPUT FORMAT (625-line and 525- line)



NOTE

14. There is a 1 line propagation delay between transferring a line from the store section to the standard register and reading it out through the OS output amplifier.

Figure 18: OUTPUT CIRCUIT SCHEMATIC

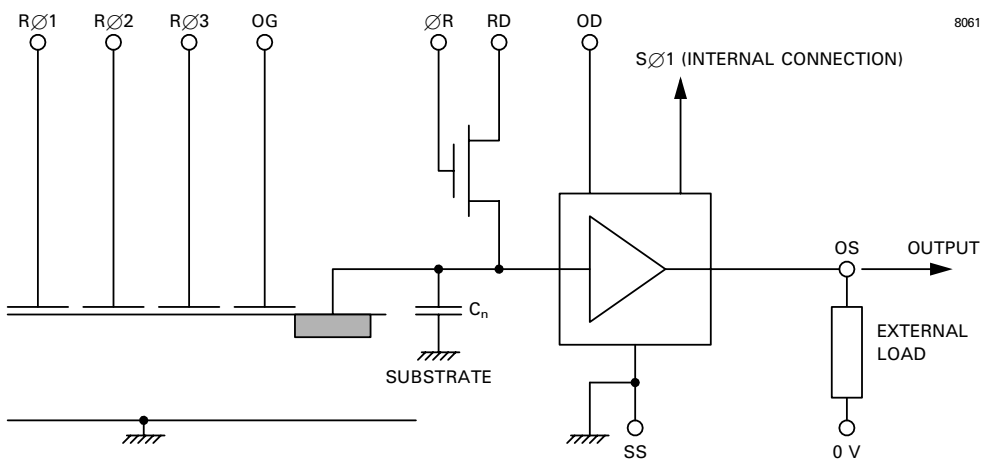
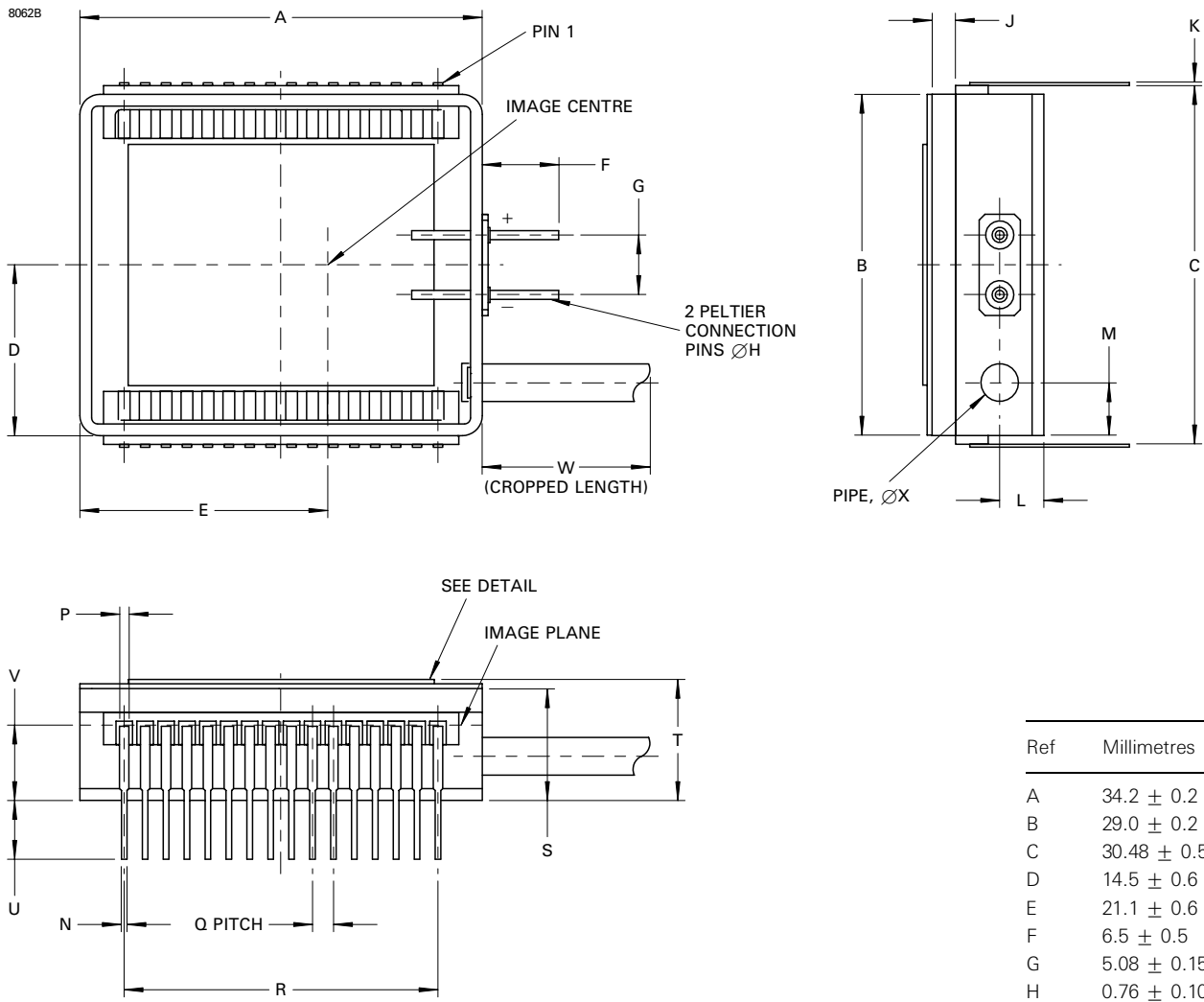
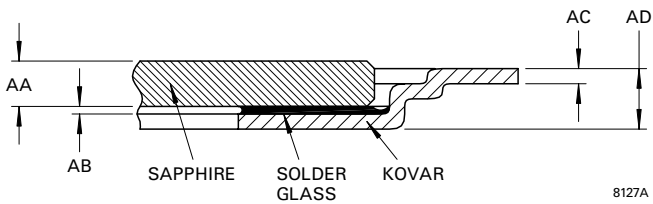


Figure 19: PACKAGE OUTLINE
 (All dimensions without limits are nominal)



Ref	Millimetres
A	34.2 ± 0.2
B	29.0 ± 0.2
C	30.48 ± 0.50
D	14.5 ± 0.6
E	21.1 ± 0.6
F	6.5 ± 0.5
G	5.08 ± 0.15
H	0.76 ± 0.10
J	2.0 ± 0.2
K	0.25 ± 0.05
L	3.75 ± 0.25
M	4.5 ± 0.2
N	0.475 ± 0.075
P	0.8 ± 0.1
Q	1.778 ± 0.130
R	26.67
S	9.5 ± 0.2
T	9.9 ± 0.4
U	4.5 min
V	6.5 ± 0.4
W	13.0 min
X	3.200 ± 0.075
AA	0.9 ± 0.1
AB	0.10 ± 0.10
AC	0.25 ± 0.03
AD	1.25 ± 0.03

Detail of Window Bonding



Outline Notes

1. Package material Fe-Ni-Co alloy.
2. The device image area is parallel to the package back surface to within 100 µm typically.
3. The sapphire window is AR coated to give a total transmission that is typically >86% between 450 and 1000 nm.

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